Amendments To the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 27 (currently amended): A processing core of a processing system for processing information using hardware-assisted context switching, comprising;

a processing unit;

an instruction cache for storing instructions for non-time-critical tasks and a code random access memory for storing instructions required for causing serving of time-critical tasks, the instruction cache and the code random access memory coupled to the processing unit;

a register group for updating status of registers related to time critical tasks; and

another register group coupled to the processing unit[;],

[a data memory and another data memory coupled to the processing unit; and

a low priority interrupt controller and a high priority interrupt controller coupled to the processing unit; and

wherein the instruction cache, the register group, the data memory, and the low priority interrupt controller are dedicated to performing non-time-critical tasks by the processing unit; and

wherein the code random access memory, the another register group, the another data memory, and the high priority interrupt controller are dedicated to performing time-critical tasks by the processing unit]

wherein the processing unit need access status of registers only in the register group for execution of time-critical tasks thereby avoiding saving and restoring status of the another registers for execution of time-critical tasks.

Claim 28 (previously presented): The processing core according to Claim 27, wherein one of the time-critical tasks is providing additional data to a video engine unit during a video compression process.

Claim 29 (previously presented): The processing core according to Claim 28, wherein the additional data is provided to the video engine unit within a time interval of less than two microseconds.

Claim 30 (previously presented): The processing core according to Claim 27, wherein one of the non-time-critical tasks is multiplexing of audio and video streams.

Claim 31 (previously presented): The processing core according to Claim 27, wherein one of the one-time-critical tasks is demultiplexing Motion Picture Expert Group (MPEG) streams.

Claim 32 (previously presented): The processing core according to Claim 27, wherein the non-time-critical tasks are user interface application.

Claim 33 (previously presented): The processing core according to Claim 32, wherein one of the user interface applications is providing an on-screen display every two seconds.

Claim 34 (currently amended): A method of processing information by a processing core for a processing system, comprising:

providing a processing unit;

coupling an instruction cache and a code random access memory to the processing unit;

coupling a register group and another register group to the processing unit;

coupling a data memory and another data memory to the processing unit;

coupling a low priority interrupt controller and a high priority interrupt controller to the processing unit;

performing non-time-critical tasks through dedicated use by the processing unit of the instruction cache, the register group, the data memory, and the low priority interrupt controller; [and]

performing time-critical tasks through dedicated use by the processing unit of the code random access memory, the another register group, the another data memory, and the high priority interrupt controller; and

accessing status of registers only in the register group for execution of time-critical tasks thereby avoiding saving and restoring status of the another registers for execution of time-critical tasks.

Claim 35 (previously presented): The method according to Claim 34, wherein performing time-critical tasks further comprises providing additional data to a video engine unit during a video compression process.

Claim 36 (previously presented): The method according to Claim 35, wherein providing additional data further comprises providing the additional data to the video engine unit within a time interval of less than two microseconds.

Claim 37 (previously presented): The method according to Claim 34, wherein performing non-time-critical tasks further comprises multiplexing of audio and video streams.

Claim 38 (previously presented): The method according to Claim 34, wherein performing non-time-critical tasks further comprises demultiplexing Motion Picture Expert Group (MPEG) streams.

Claim 39 (previously presented): The method according to Claim 34, wherein performing non-time-critical tasks further comprises performing user interface applications.

Claim 40 (previously presented): The method according to Claim 39, wherein performing user interface applications further comprises providing an on-screen display every two seconds.

Claim 41 (currently amended): An audio and video encoder/decoder, comprising:

a processing system;

a video engine unit and a video interface unit both coupled to the processing system;

an audio engine unit and an audio interface unit both coupled to the processing system and

wherein the processing system has a processing core that includes:

a processing unit;

an instruction cache for storing instructions for non-time-critical tasks and a code random access memory for storing instructions required for causing serving of time-critical tasks, the instruction cache and the code random access memory coupled to the processing unit;

a register group for updating status of registers related to time critical tasks; and

another register group coupled to the processing unit;

a data memory and another data memory coupled to the processing unit; and

[a low priority interrupt controller and a high priority interrupt controller coupled to the processing unit; and

wherein the instruction cache, the register group, the data memory, and the low priority interrupt controller are dedicated to performing non-time-critical tasks by the processing unit; and

wherein the code random access memory, the another register group, the another data memory, and the high priority interrupt controller are dedicated to performing time-critical tasks by the processing unit]

wherein the processing unit need access status of registers only in the register group for execution of time-critical tasks thereby avoiding saving and restoring status of the another registers for execution of time-critical tasks.

Claim 42 (previously presented): The audio and video encoder/decoder according to Claim 41, wherein one of the time-critical tasks is providing additional data to a video engine unit during a video compression process.

Claim 43 (previously presented): The audio and video encoder/decoder according to Claim 42, wherein the additional data is provided to the video engine unit within a time interval of less than two microseconds.

Claim 44 (previously presented): The audio and video encoder/decoder according to Claim 41, wherein one of the non-time critical tasks is multiplexing of audio and video streams.

Claim 45 (previously presented): The audio and video encoder/decoder according to Claim 41, wherein one of the non-time-critical tasks is demultiplexing Motion Picture Expert Group (MPEG) streams.

Claim 46 (previously presented): The audio and video encoder/decoder according to Claim 41, wherein the non-time-critical tasks are user interface applications.

Claim 47 (previously presented): The audio and video encoder/decoder according to Claim 46, wherein one of the user interface applications is providing an on-screen display every two seconds.